SYSTEM AND METHOD FOR DETECTING MULTIPLE DATA BIT ERRORS IN MEMORY

ABSTRACT OF THE DISCLOSURE

Detection of multiple data bit errors in physically adjacent data bits in a memory boundary having a parity bit, comprising activating each of a line of a memory boundary in a memory array having the parity bit; and, directing physically adjacent data bits in an activated line to two or more parity checking devices so that two or more physically adjacent data bits are not forwarded to the same one the two or more parity checking devices.